MOTIVATING TECHNICAL SESSION

Organized by

TnP Cell SOE, Tezpur University

SESSION ON SEMICONDUCTOR TECHNOLOGY

Mr. Harpreet S Jattana is a distinguished expert in microelectronics with over 37 years of experience. He formerly served as Scientist G/Group Head at the Semi-Conductor Laboratory, Department of Space, Government of India, leading a team of 78 scientists. His key contributions include the indigenous development of SOI-CMOS technology, high-voltage processes, and radiation-hardened VLSI technologies for space and military applications. He has played a pivotal role in advancing VLSI education in India and has contributed to numerous semiconductor initiatives under MeitY.

Mr. Harpreet S Jattana

Scientist G/Group Head – Design & Process Group,
Semi-Conductor Laboratory, Dept. of Space, Govt. Of India

Lecture Topics

- Issues and Challenges in DSM Deep Sub-Micron Devices
- Baseline CMOS Process – Steps and Integration Issues
- CMOS Manufacturing – Fab and Post-Fab Operations
- Process-Design-Fab Linkages: PDK, Usage, and QA/Reliability
- Design of Analog Components in VLSI
- Case Study: Development of a Radiation-Hardened Product

Date: March 17th & 18th, 2025

Time: 10:00 AM - 12:00 PM
03:00 PM - 05:00 PM

Venue: Dean's Gallery, SOE